## Explanation on Reaction Timer System

Project Overview: The project represents the design of a digital system aimed at creating a reaction timer game. The system integrates various components such as clock dividers, debouncers for key input, a central processing unit (CPU) for game logic, BCD converters, and display decoders for output visualization.

1. Clock Management: The system utilizes a clock divider (clk\_div) to divide a 1 ms clock into a 1 Hz clock (clk\_out\_500ms). This clock management ensures synchronization of various operations within the system. Additionally, the mili\_sec module generates a 1 ms clock (clk\_1ms\_w) from a 50 MHz input clock (clk\_50mhz), while the clk\_1sec module generates a 1 Hz clock (clk\_1hz\_w) from the 1 ms clock. These clocks are crucial for timing critical operations and ensuring the proper functioning of the system.

2. Debouncing Key Inputs: Four instances of the debouncer component are utilized to debounce the key inputs (KEYs). Debouncing ensures that the system accurately detects key presses and releases by eliminating noise and mechanical inconsistencies commonly associated with switch contacts.

3. Central Processing Unit (CPU): The heart of the system is the CPU (cpu) component, which orchestrates the game logic based on input signals and clock events. It receives clock signals, reset signals, and various player actions such as pressing keys (player\_A, player\_B), starting the game (start), and confirming targets (target\_confirm). Based on these inputs, the CPU computes scores, handles resets, and updates stimulus signals for players. It also generates outputs such as target scores, configuration enable signals, test cycles, and player scores.

4. Binary Coded Decimal (BCD) Conversion and Display: The system employs BCD converters and display decoders to represent numerical values in a human-readable format on 7-segment displays (HEX0 to HEX7). The BCD components convert binary numbers to BCD format, while the display\_decoder components translate BCD values into signals compatible with 7-segment displays. This facilitates the visualization of scores, test cycles, and other game-related information.

5. Display Handling: The disp\_process process manages the display of various messages on the LEDs (LEDs) based on certain conditions such as configuration enable or test cycles. It ensures that relevant information is displayed to the user in a clear and concise manner.

Conclusion: Overall, the project represents a comprehensive digital system design aimed at creating a game or interactive application. By integrating clock management, key debouncing, CPU logic, BCD conversion, display decoding, and display handling, the system offers a robust framework for implementing various gaming or interactive functionalities. Further testing and refinement may be necessary to ensure the proper functioning and usability of the system in real-world applications.